

Figure 1.1: IC555 Timer

**PH1C04 Electronics**

## Lecture 1: IC555 Timer

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The 555 timer (Figure 1.1) IC was introduced in the year 1970 by Signetic Corporation and gave the name SE/NE 555 timer. It is basically a monolithic timing circuit that produces accurate and highly stable time delays or oscillation. When compared to the applications of an op-amp in the same areas, the 555IC is also equally reliable and is cheap in cost. The timer IC is setup to work in either of the two modes one-shot or monostable or as a free-running or astable multivibrator. The important features of the 555 timer are:

- It operates from a wide range of power supplies ranging from + 5 Volts to + 18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilo hertz.
- The output of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- The duty cycle of the timer is adjustable.

### 1.1 Pin Configuration

The pin configuration is represented in figure 1.2. This IC consists of 23 transistors, 2 diodes and 16 resistors. The use of each pin in the IC is explained below. The pin numbers used below refers to the 8-pin DIP and 8-pin metal can packages. The circuit diagram of IC555 timer is shown in figure 1.3.

These pins are explained in detail below:

**Pin 1: Grounded Terminal:** All the voltages are measured with respect to the Ground terminal.

**Pin 2: Trigger Terminal:** The trigger pin is used to feed the trigger input when the 555 IC is set up as a

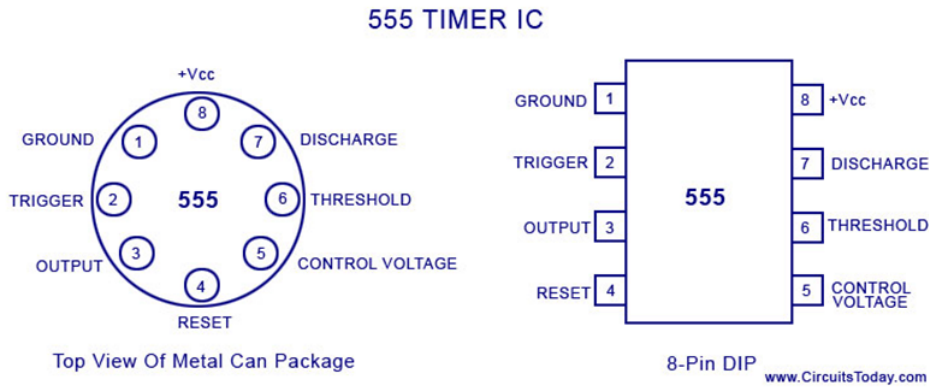


Figure 1.2: 555 Timer IC Pin Configuration

monostable multivibrator. This pin is an inverting input of a comparator and is responsible for the transition of flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. A negative pulse with a dc level greater than  $V_{cc}/3$  is applied to this terminal. In the negative edge, as the trigger passes through  $V_{cc}/3$ , the output of the lower comparator becomes high and the complimentary of Q becomes zero. Thus the 555 IC output gets a high voltage, and thus a quasi stable state.

**Pin 3: Output Terminal:** Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the normally on load and that connected between output and ground pin is called the normally off load.

**Pin 4: Reset Terminal:** Whenever the timer IC is to be reset or disabled, a negative pulse is applied to pin 4, and thus is named as reset terminal. The output is reset irrespective of the input condition. When this pin is not to be used for reset purpose, it should be connected to + VCC to avoid any possibility of false triggering.

**Pin 5: Control Voltage Terminal:** The threshold and trigger levels are controlled using this pin. The pulse width of the output waveform is determined by connecting a POT or bringing in an external voltage to this pin. The external voltage applied to this pin can also be used to modulate the output waveform. Thus, the amount of voltage applied in this terminal will decide when the comparator is to be switched, and thus changes the pulse width of the output. When this pin is not used, it should be bypassed to ground through a 0.01 micro Farad to avoid any noise problem.

**Pin 6: Threshold Terminal:** This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of  $2/3 V_{CC}$ . The amplitude of voltage applied to this terminal is responsible for the set state of flip-flop. When the voltage applied in this terminal is greater than  $2/3 V_{cc}$ , the upper comparator switches to +Vsat and the output gets reset.

**Pin 7 : Discharge Terminal:** This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

**Pin 8: Supply Terminal:** A supply voltage of + 5 V to + 18 V is applied to this terminal with respect to ground (pin 1).

The block diagram of a 555 timer is shown in the above figure. A 555 timer has two comparators, which are basically 2 op-amps), an R-S flip-flop, two transistors and a resistive network.

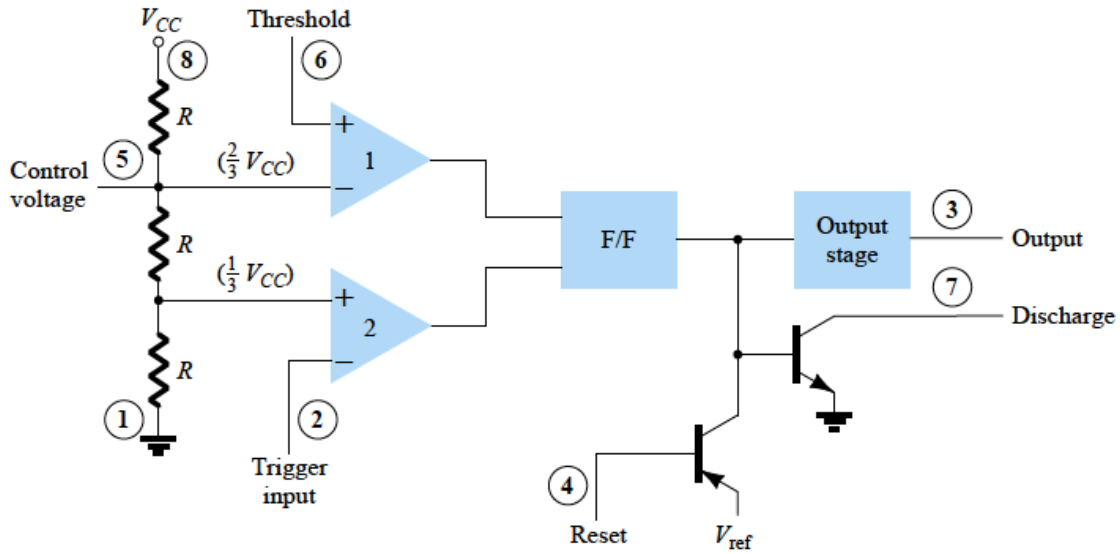


Figure 1.3: Details of 555 timer IC.

- Resistive network consists of three equal resistors and acts as a voltage divider.
- Comparator 1 compares threshold voltage with a reference voltage  $+ \frac{2}{3} V_{CC}$  volts.
- Comparator 2 compares the trigger voltage with a reference voltage  $+ \frac{1}{3} V_{CC}$  volts.
- Output of both the comparators is supplied to the flip-flop. Flip-flop assumes its state according to the output of the two comparators.

One of the two transistors is a discharge transistor of which collector is connected to pin 7. This transistor saturates or cuts-off according to the output state of the flip-flop. The saturated transistor provides a discharge path to a capacitor connected externally. Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the whole timer irrespective of any input.

## 1.2 IC555 as Monostable multivibrator

A monostable multivibrator (MMV) often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable). For auto-triggering of output from quasi-stable state to stable state energy is stored by an externally connected capacitor C to a reference level. The time taken in storage determines the pulse width. The transition of output from stable state to quasi-stable state is accomplished by external triggering. Figure 1.4 shows an monostable circuit built using an external resistor and capacitor to set the timing interval of the output signal.

Pin 1 is grounded. Trigger input is applied to pin 2. In quiescent condition of output this input is kept at  $+ V_{CC}$ . To obtain transition of output from stable state to quasi-stable state, a negative-going pulse of narrow width (a width smaller than expected pulse width of output waveform) and amplitude of greater than  $+ \frac{2}{3} V_{CC}$  is applied to pin 2. Output is taken from pin 3. Pin 4 is usually connected to  $+ V_{CC}$  to avoid accidental reset. Pin 5 is grounded through a 0.01  $\mu$ F capacitor to avoid noise problem. Pin 6 (threshold) is shorted to

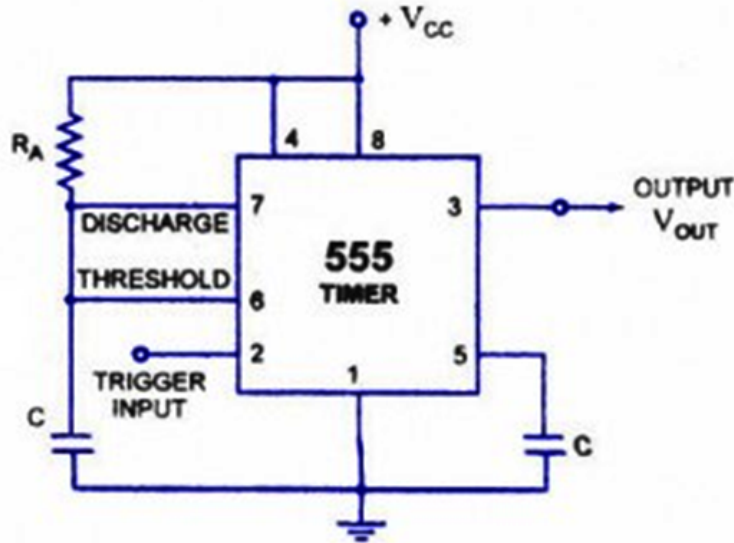


Figure 1.4: 555-timer-monostable-multivibrator.

pin 7. A resistor  $R_A$  is connected between pins 6 and 8. At pins 7 a discharge capacitor is connected while pin 8 is connected to supply  $V_{CC}$ .

#### Operation:

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor- $C$  is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below  $+1/3 V_{CC}$ , the output of comparator 2 goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor  $C$  begins charging toward  $+V_{CC}$  through resistance  $R_A$  with a time constant equal to  $R_A C$ . When the increasing capacitor voltage becomes slightly greater than  $+2/3 V_{CC}$ , the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor  $C$  and the output of the timer goes low, as illustrated in figure 1.5. The output of the Monostable Multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats. Trigger input, output voltage and capacitor voltage waveforms are shown in figure 1.5.

The output of the Monostable Multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats. Trigger input, output voltage and capacitor voltage waveforms are shown in figure. The capacitor  $C$  has to charge through resistance  $R_A$ . The larger the time constant  $R_A C$ , the longer it takes for the capacitor voltage to reach  $+2/3 V_{CC}$ .

In other words, the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as:

$$T_P = 1.0986 R_A C$$

where  $R_A$  is in ohms and  $C$  is in farads.

The above relation is derived as below. Voltage across the capacitor at any instant during charging period is given as:

$$V_C = V_{CC} (1 - \exp^{-t/R_A C})$$

Substituting  $v_c = 2/3 V_{CC}$  in above equation we get the time taken by the capacitor to charge from 0 to  $+2/3 V_{CC}$ .

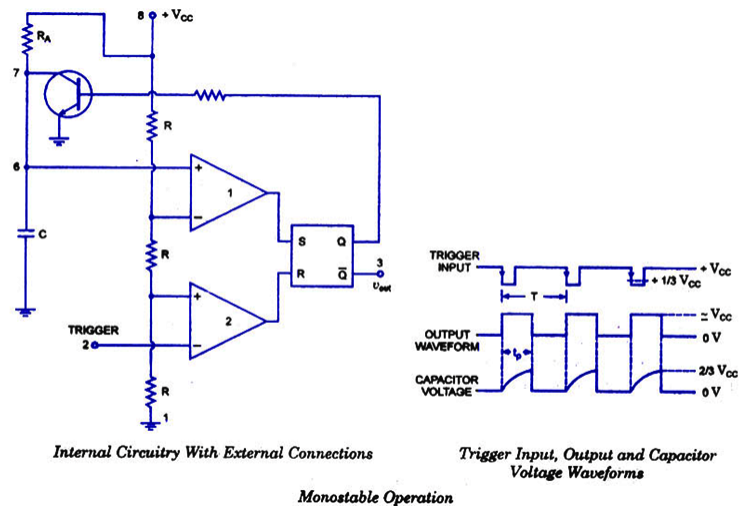


Figure 1.5: 555 monostable-multivibrator-operation.

i.e.  $+2/3V_{CC} = V_{CC} \cdot (1 - \exp^{-t/R_A C})$  or

$$t = R_A C \log_e 3 = 1.0986 R_A C$$

So pulse width,  $T_P = 1.0986 R_A C = 1.1 R_A C$ .

The pulse width of the circuit may range from micro-seconds to many seconds. This circuit is widely used in industry for many different timing applications.

### 1.2.1 Application

#### Frequency divider

It can be used as a frequency divider by adjusting the length of timing signal  $T_P$  with respect to the time period  $T$  of the trigger input signal applied to pin 2.

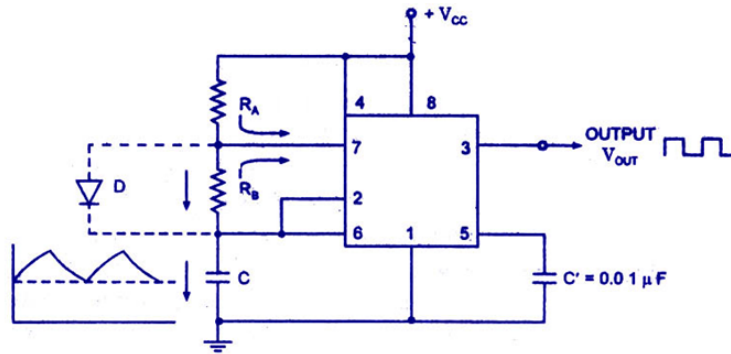
eg. To use as monostable multivibrator as a divider-by-2 circuit, the timing interval  $T_P$  must be slightly larger than the time period  $T$  of the trigger input signal. -similarly, to use the monostable multivibrator as a divider-by-3 circuit,  $T_P$  must be slightly larger than twice the period of input trigger signal.

#### Pulse stretcher

The output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of input trigger. Output pulse width of monostable multivibrator can be viewed as the stretched version of the narrow input pulse. Narrow pulse widths are not suitable for driving LED display (because its on time is infinitesimally small compared to off time. IC 555 pulse stretcher can be used to remedy this problem.

## 1.3 IC555 as Astable multivibrator

One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave generating circuit. Unlike the monostable multivibrator, this circuit does not require any external trigger to change the state of the output, hence the name free-running. An astable multivibrator can be produced by adding resistors and a



Circuit of The Timer 555 as an Astable Multivibrator

Figure 1.6: 555 Astable-multivibrator.

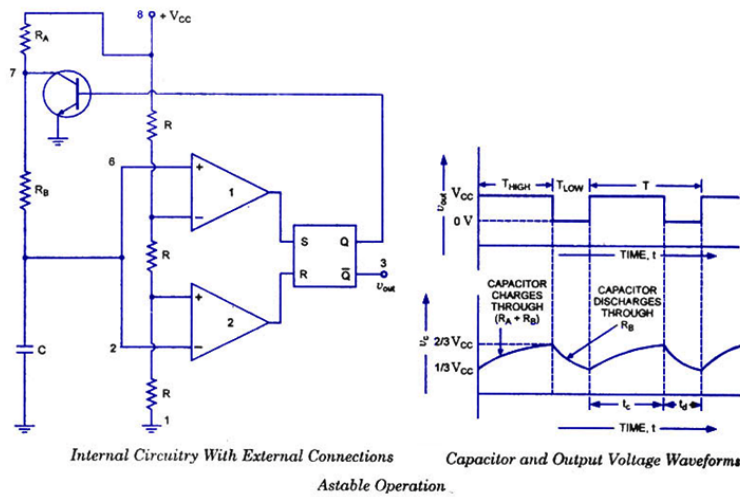


Figure 1.7: 555 Astable-multivibrator-operation.

capacitor to the basic timer IC, as illustrated in figure. The timing during which the output is either high or low is determined by the externally connected two resistors and a capacitor. The details of the astable multivibrator circuit are given in figure 1.6.

**Operation:**

In figure 1.7, when Q is low, the discharging transistor is cut-off and the capacitor C begins charging toward  $V_{CC}$  through resistances  $R_A$  and  $R_B$ . Because of this, the charging time constant is  $(R_A + R_B) C$ . Eventually, the threshold voltage exceeds  $+2/3 V_{CC}$ , the comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin 7 grounds so that the capacitor C discharges through resistance  $R_B$  with a discharging time constant  $R_B C$ . With the discharging of capacitor, trigger voltage at inverting input of comparator 2 decreases. When it drops below  $1/3 V_{CC}$ , the output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high. This proves the auto-transition in output from low to high and then to low as, illustrated in figures. Thus the cycle repeats. The time during which the capacitor C charges from  $1/3 V_{CC}$  to  $2/3 V_{CC}$  is equal to the time the output is high and is given as:  $t_c$  or  $T_{HIGH} = 0.693 (R_A + R_B) C$ , which is proved below:

Voltage across the capacitor at any instant during charging period is given as,

$$V_C = V_{CC}(1 - \exp^{-t/RC})$$

The time taken by the capacitor to charge from 0 to  $+1/3 V_{CC}$ :

$$1/3 V_{CC} = V_{CC} (1 - \exp^{-t_1/RC})$$

$$t_1 = RC \log_e 1.5 = 0.405 RC$$

Similarly, the time taken by the capacitor to charge from 0 to  $+2/3 V_{CC}$  is given by:

$$t_2 = RC \log_e 3 = 1.0986 RC \text{ So the time taken by the capacitor to charge from } +1/3 V_{CC} \text{ to } +2/3 V_{CC}:$$

$$t_c = (t_2 - t_1) = (1.0986 - 0.405) RC = 0.693 RC$$

Substituting  $R = (R_A + R_B)$  in above equation we have,

$$T_{HIGH} = t_c = 0.693 (R_A + R_B) C$$

where  $R_A$  and  $R_B$  are in ohms and  $C$  is in farads. The time during which the capacitor discharges from  $+2/3 V_{CC}$  to  $+1/3 V_{CC}$  is equal to the time the output is low and is given as:

$$t_d \text{ or } T_{LOW} = 0.693 R_B C \text{ where } R_B \text{ is in ohms and } C \text{ is in farads.}$$

The above equation is worked out as follows: Voltage across the capacitor at any instant during discharging period is given as:  $V_C = (2/3)V_{CC}\exp^{-t/R_B C}$

$$\text{Substituting } V_C = 1/3 V_{CC} \text{ and } t = t_d \text{ in above equation we have } +1/3 V_{CC} = +2/3 V_{CC}\exp^{-t_d/R_B C}$$

$$\text{Or } t_d = 0.693 R_B C$$

Overall period of oscillations,

$$T = T_{HIGH} + T_{LOW} = 0.693 (R_A + 2R_B) C$$

The frequency of oscillations being the reciprocal of the overall period of oscillations  $T$  is given as:

$$f = 1/T = 1.44 / (R_A + 2R_B) C$$

Equation indicates that the frequency of oscillation  $f$  is independent of the collector supply voltage  $+V_{CC}$ .

Often the term duty cycle is used in conjunction with the astable multivibrator.

## 1.4 IC78XX

7805 is a voltage regulator integrated circuit. It is a member of 78xx series of fixed linear voltage regulator ICs. The voltage source in a circuit may have fluctuations and would not give the fixed voltage output. The voltage regulator IC maintains the output voltage at a constant value. The xx in 78xx indicates the fixed output voltage it is designed to provide. 7805 provides  $+5V$  regulated power supply. Capacitors of suitable values can be connected at input and output pins depending upon the respective voltage levels. The pin diagram of the IC 7805 is shown in figure

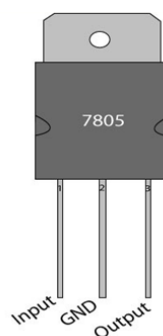


Figure 1.8: IC 7805 pin diagram.

- **Input:** In this pin of the IC positive unregulated voltage is given in regulation

- Ground: In this pin where the ground is given. This pin is neutral for equally the input and output
- Output: The output of the regulated 5V volt is taken out at this pin of the IC regulator

ICs regulator is mainly used in the circuit to maintain the exact voltage which is followed by the power supply. A regulator is mainly employed with the capacitor connected in parallel to the input terminal and the output terminal of the IC regulator. For the checking of gigantic alterations in the input as well as in the output filter, capacitors are used. While the bypass capacitors are used to check the small period spikes on the input and output level. Bypass capacitors are mainly of small values that are used to bypass the small period pulses straightly into the Earth. A circuit diagram having regulator IC and all the above discussed components arrangement revealed in the figure 1.9 below.

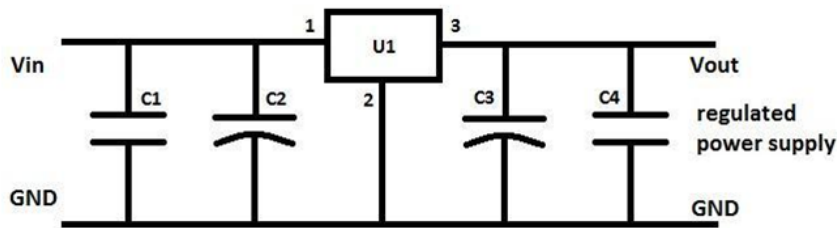


Figure 1.9: Regulated Power Supply Circuit.

- $C_1$ : This capacitor is known as bypass capacitor and is employed to bypass extremely tiny duration spikes to the ground with no distress the other components.
- $C_2$  is the filter capacitor employed to steady the slow changes in the voltage applied at the input of the circuit. Escalating the value of the capacitor amplify the stabilization as well as the declining value of the capacitor reduces the stabilization. Moreover this capacitor is not alone capable to ensure very constricted period spikes emerge at the input.
- $C_3$  is known as a filter capacitor employed in the circuit to steady the slow alterations in the output voltage. Raising the value of the capacitor enlarges the stabilization furthermore declining the value of the capacitor declined the stabilization. Moreover this capacitor is not alone capable to ensure very fine duration spikes happen at the output.
- $C_4$  is known as bypass capacitor and worked to bypass very small period spikes to the earth with no influence the other components.
- $U_1$  is the IC with positive DC and it upholds the output voltage steady exactly at a constant value even although there are major deviation in the input voltage.